Notice of Allowability	Application No.	Applicant(s)	
	10/600,885	BALLAGH ET AL.	
	Examiner	Art Unit	
	Kandasamy Thangavelu	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *October 12, 2006*.

2. ☒ The allowed claim(s) is/are *1-13*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☒ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☒ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 10/16/2006
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☒ Other *Clean copy of allowed claims*.

DETAILED ACTION

Introduction

1. This communication is in response to the Applicants' communication dated October 12, 2006. Claims 1, 5, 7, 9, 11 and 13 were amended. Claims 1-13 of the application are pending.

Examiner's Amendment

2. Authorization for this examiner's amendment was given in a telephone conversation by Mr. Justin Lou on December 8, 2006.

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to the applicants, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

3. In the Specification:

Page 3, Para 0007, L5, "that generally compliant"

has been changed to

--that are generally compliant--.

Page 6, Para 0025, L5, "data_out port 128"

has been changed to

--data_out port 138--.

Page 6, Para 0025, L5, "data_out port 128"

has been changed to

--data_out port 138--.

Page 6, Para 0026, L1, "boundary_scan_model_translator component 116"

has been changed to

--boundary_scan_model_translator component 126--.

Page 6, Para 0026, L5, "data_out port 128"

has been changed to

--data_out port 138--.

Page 7, Para 0028, L2-3, "reconfigurable hardware platform 108"

has been changed to

--reconfigurable hardware platform 110--.

4. In the claims:

Replace Claim 1 with:

1. A co-simulation system for design verification of an electronic circuit, comprising:

a high-level modeling system (HLMS);

wherein the HLMS is a software tool executable on a computing arrangement;

a boundary-scan interface coupled to the high-level modeling system and configured to translate HLMS-issued commands to signals compliant with a boundary-scan protocol;

a re-configurable hardware platform coupled to the boundary-scan interface;

a translator coupled to the boundary-scan interface, implemented on the re-configurable hardware platform, and configured to translate input signals compliant with the boundary-scan protocol to signals compliant with a second protocol;

a first component instantiated within a wrapper component, wherein the wrapper component is coupled to the translator and is configured to transfer input signals of the second protocol to the first component; and

a second component co-simulated by the HLMS in software while the first component is co-simulated on the reconfigurable hardware platform;

wherein the HLMS-issued commands include at least one command that forces input co-simulation data from the second component to the first component, and/or at least one command that extracts output co-simulation data from the first component for input to the second component.

In amended claim 3, Line 3, L5, "the component"

has been changed to

--the first component--.

Replace Claim 5 with:

5. A system for interfacing a high-level modeling system (HLMS) with a hardware platform for co-simulation of a first component on the hardware platform for design verification of an electronic circuit, comprising:

an interface coupled to the HLMS and configured to translate HLMS-issued commands to signals compliant with a boundary-scan protocol, and translate signals compliant with the boundary-scan protocol to data compatible with the HLMS;

wherein the HLMS is a software tool executable on a computing arrangement;

wherein the HLMS-issued commands include at least one command that forces input co-simulation data from a second component to the first component, and/or at least one command that extracts output co-simulation data from the first component for input to the second component;

wherein the second component is co-simulated by the HLMS in software while the first component is co-simulated on a reconfigurable hardware platform;

a translator coupled to the interface, implemented on the re-configurable hardware platform, and configured to translate input signals compliant with the boundary-scan protocol to signals compliant with a second protocol, and translate output signals compliant with the second protocol to signals compliant with the boundary-scan protocol; and

a wrapper component implemented on the re-configurable hardware platform, the wrapper component coupled to the translator and being configured for instantiation of the first component

within the wrapper component and configured to transfer input signals of the second protocol to the first component and transfer output signals of the second protocol to the translator.

Replace Claim 9 with:

9. A method for interfacing a high-level modeling system (HLMS) with a reconfigurable hardware platform for design verification of an electronic circuit, comprising:

co-simulating a first component on the reconfigurable hardware platform in hardware while co-simulating a second component on the HLMS;

wherein the HLMS is a software tool executable on a computing arrangement;

coupling an interface to the HLMS, wherein the interface is configured to translate signals compliant with a boundary-scan protocol to data compatible with the HLMS;

wherein the interface further translates HLMS-issued commands to signals compliant with the boundary-scan protocol, and the HLMS-issued commands include at least one command that forces input co-simulation data from the second component to the first component, and/or at least one command that extracts output co-simulation data from the first component for input to the second component;

configuring the reconfigurable hardware platform with a translator and a wrapper component coupled to the translator; and

coupling the translator to the interface, wherein the translator is configured to translate signals compliant with a second protocol to signals compliant with the boundary-scan protocol;

wherein the wrapper component is configured for instantiation of the first component within the wrapper component and configured to transfer signals of the second protocol to the translator.

Replace Claim 13 with:

13. An apparatus for interfacing a high-level modeling system (HLMS) with a reconfigurable hardware platform for design verification of an electronic circuit, comprising:

means for co-simulating a first component on the reconfigurable hardware platform in hardware while co-simulating a second component on the HLMS;

wherein the HLMS is a software tool executable on a computing arrangement;

means for coupling a boundary-scan interface to the HLMS, wherein the boundary-scan interface is configured to translate HLMS-issued commands to signals compliant with a boundary-scan protocol, and translate signals compliant with the boundary-scan protocol to data compatible with the HLMS;

wherein the HLMS-issued commands include at least one command that forces input co-simulation data from the second component to the first component, and/or at least one command that extracts output co-simulation data from the first component for input to the second component;

means for configuring the reconfigurable hardware platform with a translator and a wrapper component coupled to the translator;

means for coupling the translator to the boundary-scan interface, wherein the translator is configured to translate input signals compliant with the boundary-scan protocol to signals

compliant with a second protocol, and translate output signals compliant with the second protocol to signals compliant with the boundary-scan protocol; and

means for configuring the wrapper component to instantiate the first component within the wrapper component, and means for transferring input signals of the second protocol to the first component and for transferring output signals of the second protocol to the translator.

A clean copy of the allowed claims is attached.

Examiner's Amendment for drawing errors

5. The following changes to the drawings have been approved by the examiner and agreed upon by applicant: See the agreed upon changes to Fig. 1 indicated by the red marked corrections.

In order to avoid abandonment of the application, applicant must make these above agreed upon drawing changes.

Reasons for Allowance

6. Claims 1-13 of the application are allowed over prior art of record.

7. The following is an Examiner's statement of reasons for the indication of allowable subject matter:

The closest prior art of record shows:

(1) a co-simulation system for pure software simulation and pure hardware emulation/acceleration of an integrated circuit; an inter-chip communication system transfers signals across FPGA chip boundaries only when these signals change values; a reconfigurable computing system contains a software model of the user design; a reconfigurable hardware array contains the hardware model of the user design that is implemented in reconfigurable logic elements; FPGAs are used in the reconfigurable board to model the hardware portion of the user's design; the system has functionality to debug the software portion and the hardware portion of the user's design; the user can simulate the circuit design using the software simulation, accelerate the test/debug process using the hardware model, return to the simulation portion, and return to the hardware acceleration until the test/debug process is complete; there is the ability to switch between the software simulation and hardware acceleration; the FPGA controller includes boundary scan test interface that provides JTAG implementation to externally check a system's logic units; the control logic receives a signal and translates into a control signal; a device driver provides an interface between the computing environment and the reconfigurable hardware unit; the interface includes bi-directional communication handshake signals (**Tseng et al.,** U.S. Patent Application 2006/0117274);

(2) a simulation/emulation server system that is capable of allocating multiple resources to multiple hosts; a RCC computing system contains the computational resources to allow the user to simulate the user's software modeled design in software and control the hardware

acceleration of the hardware modeled portion of the design; the RCC hardware accelerator contains the reconfigurable array of logic elements that model at least a portion of the user's design in hardware so that user can accelerate the debugging process; the RCC computing system is tightly coupled to the RCC hardware accelerator via a software clock; the RCC system can also be used for emulation purposes; the hardware resources include slots of one or more boards of FPGA chips for reconfigurably loading the user design as a hardware model; when a host or several hosts request access to certain slots, an arbiter determines the winning host and assigns the slots to the winning hosts; to communicate with the server, the host stations include control logic to deliver a request to the simulation server; the request includes a command type and slot number (**Lin,** U.S. Patent Application 2004/0236556); and

(3) a method for co-simulating a digital circuit using a high-level HDL to achieve faster simulation speeds; the method uses a simulation engine that communicates with one first programming language by means of a foreign language interface and communicates directly with a second programming or hardware description language; a portion of the digital circuit is modeled in a high-level hardware description language; the model is converted to a software model in the first programming language; a portion of the digital circuit is modeled in a second programming language; the software model in the first programming language and the model in the second programming language are run in the simulation engine; a high level sequential description of the hardware model is generated automatically from the high level hardware description; this achieves high level HDL simulation for co-simulation of a high level hardware description; the method co-simulates a hardware circuit described as an algorithm in a high level language (**Zammit et al.,** U.S. Patent Application 2002/0083420).

None of these references taken either alone or in combination with the prior art of record discloses a co-simulation system for design verification of an electronic circuit, specifically including:

(Claim 1) "a boundary-scan interface coupled to the high-level modeling system and configured to translate HLMS-issued commands to signals compliant with a boundary-scan protocol;

a translator coupled to the boundary-scan interface, implemented on the re-configurable hardware platform, and configured to translate input signals compliant with the boundary-scan protocol to signals compliant with a second protocol".

None of these references taken either alone or in combination with the prior art of record discloses a system for interfacing a high-level modeling system (HLMS) with a hardware platform for co-simulation of a first component on the hardware platform for design verification of an electronic circuit, specifically including:

(Claim 5) "an interface coupled to the HLMS and configured to translate HLMS-issued commands to signals compliant with a boundary-scan protocol, and translate signals compliant with a boundary-scan protocol to data compatible with the HLMS;

a translator coupled to the interface, implemented on the re-configurable hardware platform, and configured to translate input signals compliant with the boundary-scan protocol to signals compliant with a second protocol, and translate output signals compliant with the second protocol to signals compliant with the boundary-scan protocol".

None of these references taken either alone or in combination with the prior art of record discloses a method for interfacing a high-level modeling system (HLMS) with a reconfigurable hardware platform for design verification of an electronic circuit, specifically including:

(Claim 9) "coupling an interface to the HLMS, wherein the interface is configured to translate signals compliant with a boundary-scan protocol to data compatible with the HLMS;

wherein the interface further translates HLMS-issued commands to signals compliant with the boundary-scan protocol;

coupling the translator to the interface, wherein the translator is configured to translate signals compliant with a second protocol to signals compliant with the boundary-scan protocol".

None of these references taken either alone or in combination with the prior art of record discloses an apparatus for interfacing a high-level modeling system (HLMS) with a reconfigurable hardware platform for design verification of an electronic circuit, specifically including:

(Claim 13) "means for coupling a boundary-scan interface to the HLMS, wherein the boundary-scan interface is configured to translate HLMS-issued commands to signals compliant with a boundary-scan protocol, and translate signals compliant with the boundary-scan protocol to data compatible with the HLMS;

means for coupling the translator to the boundary-scan interface, wherein the translator is configured to translate input signals compliant with the boundary-scan protocol to signals compliant with a second protocol, and translate output signals compliant with the second protocol to signals compliant with the boundary-scan protocol".

8. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 571-272-3717. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez, can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to TC 2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K. Thangavelu
Art Unit 2123
December 8, 2006

12/8/06

PAUL RODRIGUEZ
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

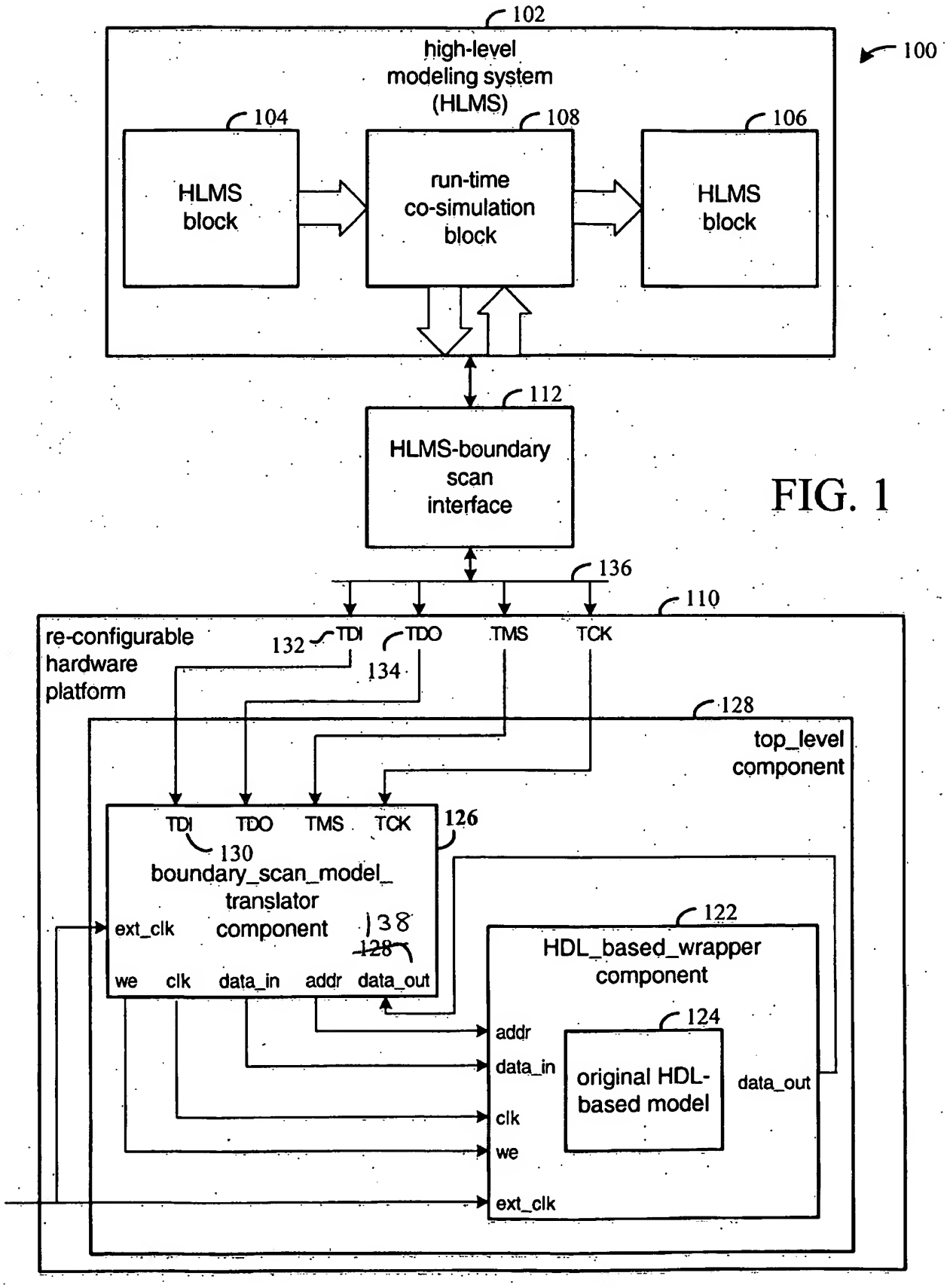
102
high-level
modeling system
(HLMS)
100
104
HLMS
block
108
run-time
co-simulation
block
106
HLMS
block
112
HLMS-boundary
scan
interface
136
110
re-configurable
hardware
platform
132
TDI
TDO
TMS
TCK
134
128
top_level
component
TDI
TDO
TMS
TCK
126
130
boundary_scan_model_
translator
component
ext_clk
138
128
we
clk
data_in
addr
data_out
122
HDL_based_wrapper
component
124
addr
data_in
clk
we
ext_clk
original HDL-
based model
data_out

FIG. 1